UNITED STATES PATENT APPLICATION

FOR

NEW PEAK HOLD SCHEME

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FIELD OF THE INVENTION

The present invention relates generally to peak detectors and more particularly to a peak detector for a small input signal.

BACKGROUND OF THE INVENTION

In disks, such as DVD or DVD-RAM, information is recorded in sector units. A sector includes a header information area having a physical identification data and a user data area. The header information area is typically divided into a peak header area and a bottom header area, and user data is divided into land area and groove area. In DVD-RAM disks, a track is formed spirally, and the track is shifted laterally at a predetermined reference point. The reference point usually becomes a starting point of the first sector.

In DVD applications, peak detectors are used. An AC peak detector is non-linear circuit used to obtain a steady state amplitude at a level of the peak amplitude of the input AC signal. The input AC signal need not be a uniform sinusoidal or an infinite sum of sinusoidals such as in a square wave signal, but any signal with approximately complimentary positive and negative voltage peaks, such as communication data signal can be an AC signal.

A number of peak detector designs are known, however, each design has shortcomings which limit the range of operability and performance within that range. In particular, there is a need for peak detectors which detect peaks with amplitudes as low as 50 or even 20 millivolts. The known designs do not demonstrate acceptable

performance at such levels and more particularly has dead zones where a new peak is not recorded.

Figure 1 illustrates a peak hold circuit. An input signal is input to the base of transistor 100. A current flows from collector to base of collector 100. If the current exceeds the current flowing in the constant current source 102, current flows through capacitor 104 and charges up capacitor 104. The voltage on capacitor 104 is the peak hold voltage.

Figure 2 illustrates a typical input voltage. As discussed before, the input signal need not be sinusoidal. Figures 2 and 3 illustrates wave forms including the held voltage at the top of the wave form.

Figure 3 illustrates the relationship between the input amplitude and the peak hold voltage and the input amplitude. As can be very clearly seen, this circuit introduces a large amount of dead region that is not representative of the peak voltage.

SUMMARY OF THE INVENTION

The present invention provides a peak hold circuit that includes a track and hold circuit and a comparator circuit which provide improved peak detection with minimal dead regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a peak hold circuit.

Figure 2 illustrates an input signal.

Figure 3 illustrates a wave form showing the relationship between peak hold voltage/input amplitude and input amplitude.

Figure 4 illustrates a peak hold circuit of the present invention.

Figure 5 illustrates a wave form showing the relationship between peak hold voltage/input amplitude and input amplitude of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

Turning to Figure 4, an input signal which may be the input signal of Figure 2 is input to a track and hold circuit 400 through input terminal 410. The hold circuit tracks the input signal and holds it and outputs an output signal in accordance with a clock signal which is input. The output of the track and hold circuit 400 is input to capacitor 406, and capacitor 406 is connected to the track and hold circuit 400 and connected to ground. Connected in parallel to the capacitor 406 is constant current source 404. The constant current source 404 is connected to the track and hold circuit 400 and connected in parallel to the capacitor 406. The capacitor 406 forms a voltage from the charge resulting from the output of the track and hold circuit 400 and produces a peak hold voltage as an output voltage. The output of the track and hold circuit 400 is connected to the minus input of comparator 408. Additionally, the input signal is connected to the plus input of comparator 408. The output of comparator 408 is a series of pulses and is input to the clock input of the track and hold circuit 400.

In operation, the input signal is input to the track and hold circuit 400 as well as the comparator 408. The output from the track and hold circuit which corresponds to the current or old peak old voltage is input to the comparator, and a comparison is made within comparator 408 to compare the new peak with the old peak voltage. The comparator 408 produces an output pulse whenever the input signal is greater than the current or old peak voltage. This output from the comparator 408 is a series of pulses which is input to the clock input of the track and hold circuit 400. Thus, the track and hold circuit outputs the input voltage in accordance with the output of the comparator circuit 404. The peak hold voltage is formed on capacitor 406 and is held. During non-clock pulses, the voltage of capacitor 406 is discharged through current source 404. The present invention provides a high peak hold voltage for input amplitude as illustrated in Figure 5 with a small amount of dead region.